REMARKS

In the Office Action dated March 4, 2003, the Examiner rejected claims 1 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,920,084; rejected claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Wakai et al. (USP 5,003,356), in view of Hughes et al. (USP 5,591,676)

By this Amendment, Applicant cancels claim 1 and adds new claims 23-32. Accordingly, claims 23-32 are pending in this application.

Claims 23-26 are allowable over the cited references in that these claims recite a combination of features including, for example, disposing and patterning an array of substantially transparent pixel electrodes on said substrate over said insulating layer so that the patterned pixel electrodes overlap said gate and drain lines in order to increase the display's pixel aperture ratio, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes to one of the gate and drain lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Claims 27 and 28 are allowable over the cited references in that these claims recite a combination of features including, for example, forming an array of substantially transparent pixel electrodes on said substrate over said insulating layer so that the pixel electrodes overlap said address lines in order to increase the display's pixel aperture ratio, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes to one of the address lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Claims 29-32 are allowable over the cited references in that these claims recite a combination of features including, for example, forming an array of pixel electrodes over the

insulating layer and overlapping the gate and drain address lines, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes to one of the gate and drain address lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Therefore, Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

Should the Examiner deem that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at 202 496-7413.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: September 3, 2003

Respectfully submitted,

By_____

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